REMARKS

Claims 1-16 were pending in the present application. By virtue of this response, claims 2, 3, 5 and 6 have been amended, no claims have been cancelled, and no new claims have been added. Accordingly, claims 1-16 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented. No new matter has been added.

Information Disclosure Statement

Applicant thanks the Examiner for considering the Information Disclosure Statement of January 15, 2004. The Applicant would also like to point out that the Examiner cited Document number US-5,966,322 to Pohm et al. on the Notice of References Cited for the Office Action of January 7, 2005. The Applicant believes that this was an error, and that the reference indicated should properly have been US-US 5,966,332 to Takano. To be certain that the Applicant has adequately responded to all of the references raised by the Examiner, Applicant respectfully requests clarification.

Claim Objections

The Office Action objected to the phases "first monitor cells" and "second monitor cells." Office Action of January 7, 2005, page 3. Claims 2, 3, 5 and 6 have been amended to recite "first monitor cell" and "second monitor cell," as suggested by the Office Action. This amendment was done merely to clarify the antecedent basis of the phase "at least a first monitor cell and a second monitor cell," as recited in claim 2, and was not otherwise done for reasons of patentability.

Rejections under 35 U.S.C. §112

Claim 2 stands rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. According to the Office Action:

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> "... the phrase 'or a second monitor cell' renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by 'or'), thereby rendering the scope of the claim(s) unascertainable." Office Action of January 7, 2005, page 3.

By virtue of this response, Applicant has amended claim 2 to recite "at least a first monitor cell and a second monitor cell." Thus, the indefiniteness rejection of claim 2 under 35 U.S.C. §112 has been rendered moot. Applicant respectfully requests withdrawal of this rejection.

Rejections under 35 U.S.C. §102(b)

Claims 1-2 stand rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,966,332 to Takano ("Takano"). According to the Office Action:

> "Regarding claims 1-2, Takano discloses a semiconductor memory device (Figure 10) comprising: a plurality of memory cells (122), each of which is capable of storing N-level data (N represents a natural number of 2 or greater) and being reprogrammed; a plurality of *monitor cells* (Col 14, lines 12-20) *that separately store individual data values of the N-level data by using the same scheme as that used by the memory cells*..." Office Action of January 7, 2005, page 4, emphasis added.

Applicant respectfully disagrees.

Takano does not describe a plurality of monitor cells that separately store individual data values of the N-level data by using the same scheme as that used by the memory cells, as recited by claims 1 and 2. Instead, Takano describes an array of memory cells (122) that can be controlled so that at least one memory cell in the array may be erased in a "memory cell by memory cell" format. See Takano, abstract. Nowhere does Takano show or describe *monitor cells*, particularly monitor cells that separately store individual data values of the N-level data by using the same scheme as that used by the memory cells.

The Office Action points to Col 14, lines 12-20 of Takano to indicate that Takano describes monitor cells. However, this portion of Takano describes *sense amplifiers* that are used to monitor the progression of the erasure of memory cells. See Takano, col 14, lines 12-20 ("In step

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15, the *sense amplifiers* connected to the respective bit lines BLm-BLt *monitor the cell currents* flowing through the eight memory cells 101 associated with the bit lines BLm-BLt. Monitoring in this manner *allows the progression of erasure of the memory cells to be detected.* In step 16, when the cell current of each memory cell 101 detected by the associated sense amplifier reaches a predetermined value, the control core circuit 132 controls the column decoder 124 to terminate the erasing operation," emphasis added).

Takano's sense amplifiers are not monitor cells that store individual data values of the N-level data by using the same scheme as that used by the memory cells, as recited by claims 1 and 2. According to Takano, sense amplifiers discriminate the level of current flowing in an associated memory cell. Takano, col. 7, lines 41-43. These sense amplifiers are not storage cells and do not store data. Instead, the sense amplifiers detect and monitor current flowing through a memory cell during erasure, to permit detection of the progression of the erasure process. Takano, col. 13, lines 34-45.

In order to anticipate, a reference must teach every aspect of the claimed invention either explicitly or impliedly. MPEP §706.02. Since Takano does not show or describe monitor cells that separately store individual data values of the N-level data by using the same scheme as that used by the memory cells, as recited by claims 1 and 2, Takano cannot anticipate the pending claims. Thus, the Applicant respectfully requests withdrawal of the 35 U.S.C. §102(b) rejection of claims 1 and 2.

Allowable Subject Matter

The Applicant thanks the Examiner for indicating that claims 12-16 are allowed, and that claims 3-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent claims. However, in light of the amendments and remarks herein, Applicant respectfully asserts that all of the pending claims, 1-16 are allowable.

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CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no.559502000300 . However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: 5.4.05

Respectfully submitted,

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